IN THE SPECIFICATION:

Page 26, second full paragraph, please amend as follows:

If a signal line for supplying a ~~eoek~~ clock is close to a normal signal line, the power supply may similarly cause noise in the former signal line, which may thus become defective. In this case, the fault list is ordered in such a manner similar to that described above, by providing the layout device with information on the signal line for supplying a clock.

Page 40, third full paragraph, please amend as follows:

~~An~~ A detection device called a "tester" is generally used to perform detection for faults in a semiconductor integrated circuit. Information including time, a signal status, and a signal detecting terminal which is output by the tester when the semiconductor integrated circuit malfunctions is collectively called a "fail log". As described below, it is a main object of the present invention to simply and accurately extract suspected failing sites from a netlist in a relatively short time by

changing ~~measuring conditions~~ testing condition in the tester to modify a fail log, comprehensively analyzing a plurality of fail logs, or adding physical layout information on the mask layout and wiring.

Page 44, first full paragraph, please amend as follows:

In this manner, when the measuring voltage is changed, the failing sites change and increase to change the output results (the fail log). In this case, since the fail log obtained at a voltage of 3 or 3.5 V arises from a plurality of failing sites, if this fail log is used with the current system, a large amount of time may be required to deduction the failing sites, resulting in incorrect identification. On the other hand, at 2.5 V, corresponding to a boundary condition under which a failing site appears in the fail log in FIG. 39, only the effect of one fault at the point A in FIG. 2 appears in the fail log, so that the failing sites can be easily sorted out using the current system. During the process, the tester 801 varies the ~~measuring conditions,~~ testing conditions, and a fail log

processing means 802 detects the boundary condition to output the current fail log 803, which is passed to a failing site storage means 810. The ~~measuring conditions~~ testing condition may include temperature, frequency, and the like in addition to voltage.

Page 44 line 27 to Page 43, line 18, please amend as follows:

FIGS. 41 and 42 show a second example of identification of suspected failing sites by the above described fault diagnosis system 904. Various faults occur in a semiconductor integrated circuit, and fail logs output as a result of tester measurements thus have a certain tendency. If, for example, the fail log does not vary despite variations in frequency, a fault independent of frequency, for example, a degenerative fault is guessed. On the contrary, if the fail log varies when the frequency is varied, a fault dependent on frequency, for example, crosstalk is guessed. On the other hand, if the fault depends on the ~~measuring conditions,~~ testing condition, a

plurality of parameters may affect it. In this case, the fault is assumed to depend on these parameters. If a fault results from, for example, a minor current leakage, it affects both measured voltage and temperature parameters. Accordingly, the possibility of minor leakage can be estimated by checking fail logs obtained at different ~~measuring conditions.~~testing condition. If an identical fail log is obtained with a plurality of parameters, an identical failing site is assumed to be detected.

Page 46, line 1 to Page 47, line 18, please amend as follows:

FIG. 41 shows a process flow. In this process, the ~~measuring conditions~~ testing condition are varied in the tester 801, which uses two parameters such as the parameters A and B, and a fail log processing means 4501 determines dependency on the ~~measuring conditions~~ testing condition to output the result of the determination and a fail log for the boundary condition if the result is affirmative or an invariable fail log if the

result is negative. The result of the determination and a fail log 4502 for the parameter A and the result of the determination and a fail log 4503 for the parameter B which are all output by the fail log processing means 4501 are used as an input, and diagnosis means 4504 compares these determination results and fail logs together to guess the types of likely faults from a fault table 4505 in the form shown in FIG. 42 (4506), the fault table being held as a database. If the fail logs are exactly the same, information indicating the match is also output. In this manner, the type and site of the fault can be guessed from the fail log information from the tester.

FIG. 43 shows a third example of a method by which the fault diagnosis system 904 sorts out suspected failing sites. Again, a method with two parameters such as the parameters A and B will be explained. The ~~measuring conditions~~ testing condition are varied in the tester 801, and the fail log processing means 4501 determines dependency on the ~~measuring conditions~~ testing condition to output the result of the determination and a fail log for the boundary condition if the result is affirmative or an invariable fail log if the result is negative. The result of

the determination and the fail log 4502 for the parameter A and the result of the determination and the fail log 4503 for the parameter B which are all output by the fail log processing means 4501 are used as an input, and a diagnosis/fail log processing means 4601 compares these determination results and fail logs together to guess the types of likely faults from the fault table 4505 in the form shown in FIG. 42 (4603), the fault table being held as a database. The diagnosis/fail log processing means 4601 comprehensively analyzes the fail logs 4502 and 4503 to extract duplicates from the fail logs to generate a fail log 4602 and passes it to a failing site storage means 4101 of the fault diagnosis system to deduction suspected failing sites. Thus, since the required information is obtained from the fail logs to guess the types and sites of faults in order to comprehensively analyze the fail logs for a plurality of ~~measuring conditions,~~ testing condition, the fault diagnosis system can subsequently efficiently deduction suspected failing sites and improve diagnosis accuracy.

Page 50, line 14 to Page 51, line 9, please amend as follows:

FIG. 47 is a diagram useful in explaining a method for detecting faults in the semiconductor integrated circuit, the method sorting out failing sites by varying the ~~measuring conditions~~ testing condition in the tester to comprehensively analyze fail logs for the plurality of ~~measuring conditions~~ testing condition and adding physical layout information on the mask or wiring layout to guess and order suspected faults with their likelihood. In this case, failing sites are sorted out by varying the ~~measuring conditions~~ testing condition in the tester 801 to comprehensively analyze fail logs for the plurality of ~~measuring conditions~~ testing condition (4501) and adding physical layout information 903 on the mask or wiring layout obtained from the layout means 902, to guess and order suspected faults with their likelihood (910). Fail log information 4602 is stored in the failing site storage means 4101. The suspected fault ordering means 910 uses the suspected faults in the initial suspected fault storage means 4105 as an input to order

them, and the failing sites are passed to the failing site deduction means 106 in accordance with this order. As described above, by comprehensively analyzing the fail logs for the plurality of ~~measuring conditions~~ testing condition set in the tester 801 and adding the physical information on the mask layout or wiring, the types of the suspected faults can be efficiently guessed and the failing sites can be efficiently sorted out.